

## DEPARTMENT OF PHYSICS MAR THOMA COLLEGE FOR WOMEN, PERUMBAVOOR

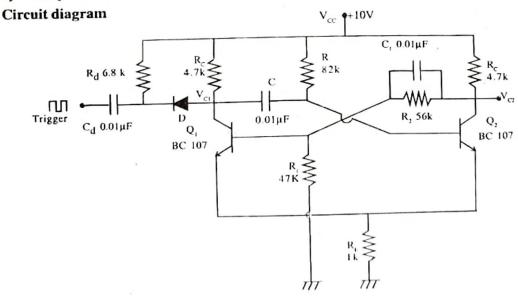
#### **MONOSTABLE MULTIVIBRATOR**

Aim: To set up and study a monostable multivibrator using transistors.

Components and equipments required Transistors, resistors, capacitors, signal generator, de power source, bread board and CRO.

**Theory** This multivibrator has only one stable state as its name suggests. It has one quasi-stable state also. An external trigger forces this circuit to go to quasi-stable state from its stable state and remain in that state for an amount of time determined by the discharging time of the capacitor. R and C are the timing elements and C, is the speed up capacitor.

Figure shows a monostable multivibrator using single bias supply. As soon as the power supply is switched ON, transistor  $Q_1$  goes to cut off state and  $Q_2$  goes to saturation state due to regenerative action. The stable state voltages are  $V_{c1} = V_{c2}$ ,  $V_{c2} = V_{cE}$  (sat),  $V_{B1} = -V_f$ , and  $V_{B2} = V_{mE}(sat)$ . The moment a negative trigger is applied at the collector of the transistor  $Q_1$ , transistor  $Q_2$  goes to cut off state. Hence  $V_{c2}$  jumps to  $V_{c2}$ . This sudden change is coupled to the base of the transistor  $Q_1$  and hence it goes to ON state. The collector voltage of the transistor  $Q_1$  suddenly drops by an amount  $I_{c1}R_{c1}$ , where  $I_{c1}$  is the current through the resistance  $R_{c1}$ . Since capacitor acts as a short circuit for a sudden change, the base voltage of  $Q_2$  suddenly drops by an equal amount. Now the polarity of the charge of the capacitor is such a way that the negative is at its right side. Now capacitor charges from this negative potential to  $+V_{c2}$  through R and  $Q_1$ . Capacitor discharges through the ON transistor. Once it becomes zero it further charges towards  $V_{c2}$ . But, when the positive potential at the right side of the capacitor reaches the cut in voltage,  $Q_2$  turns ON. Thus the circuit comes back to the stable state. It will continue till the next trigger comes at the base of  $Q_2$ . The time duration of the quasi-stable state is given by the expression T = 0.69 RC.





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Design Output requirements Amplitude = 10 V, pulse width = 1ms. Selection of transistor and diode Choose transistors BC 107 and diode 1N4001.

DC bias conditions  $V_{CC} = 10 \text{ V}, V_{RE} = 2 \text{ V}$ 

Design of  $R_E R_E = V_{RE} / I_E = 1 \text{ k}$  Since  $I_E = I_C$ 

Design of  $R_1$  and  $R_2$  Consider the astable state  $(Q_1$  is OFF and  $Q_2$  is ON)

Assume  $V_{BE} = -1 \text{ V}$  to assure that the transistor is in cut off state. Then  $V_{BI} = 2 - (-1) = 1 \text{ V}$ . Since  $I_{BI} = 0$ , current flowing through  $R_2$  = current flowing through  $R_3$ 

$$V_{B1} = \frac{V_{C2} R_1}{R_1 + R_2} = \frac{2.3 \text{ V} \times R_1}{R_1 + R_2}$$

From this,  $R_2 = 1.3 R_1$ 

Consider the astable state  $(Q_1 \text{ is ON and } Q_2 \text{ OFF})$ :

$$V_{C2} = 12 \text{ V since } Q_2 \text{ is OFF.}$$

$$V_{B1} = V_{BEsat} + V_{RE} = 2.8 \text{ V}$$

Also, 
$$I_{R2} = I_{B1} + I_{R1}$$

i.e., 
$$\frac{12 \text{ V} - 2.8 \text{ V}}{R_2} = I_{B1} + \frac{2.8 \text{ V}}{R_1}$$

Substituting the value of R, we get  $9.2 \text{ R}_1 = 1.3 \times 10^{-4} \times \text{R}_1^2 + 3.64 \times \text{R}_1$ 

or 
$$1.3 \times 10^{-4} \times R_1^2 - 5.56 \times R_1 = 0$$

Solving this quadratic expression

$$R_1 = + \frac{-5.56 \pm \sqrt{31}}{2 \times 1.3 \times 10^{4} \times R_1^2} = 42.8 \text{ k. Use } 47 \text{ k std.}$$

Then  $R_2 = 55.64 \text{ k}$  use 56 k std.

Design of  $R_{C1}$  and  $R_{C2}$   $R_C = \frac{V_{CC} - V_C}{I_C sat} = 4.35 \text{ k. Use } 4.7 \text{ k std.}$ 

Take 
$$R_{C1} = R_{C2} = R_{C}$$

Design of R R must be able to provide base current enough to keep the transistors in saturation.

$$I_{\rm B} \, \text{min} = I_{\rm c} / h_{\rm FE} = 2 \, \text{mA} / h_{\rm FE} = 20 \, \mu \text{A}$$

Consider an over-driving factor 5, so that transistor will be indeed in saturation.

Then actual base current  $I_B = 5 I_B \min = 0.1 \text{mA}$ 

$$R = (V_{CC} - V_{BE} \text{ sat}) / 0.1 \text{ mA} = 73 \text{ k. Use } 82 \text{ k.}$$

We have T = 0.69RC. substituting the value of R we get,  $C = 0.01 \mu F$ .

Design of differentiator circuit: The condition is  $R_d C_d < 0.0016 T_t$ , where  $T_t$  = time period of trigger signal. To avoid the loading of the signal generator by the differentiator, take  $R_d = 6.8$  k.

Let 
$$T_t$$
 be 2 ms. Then  $C_d = 0.01 \mu F$ .

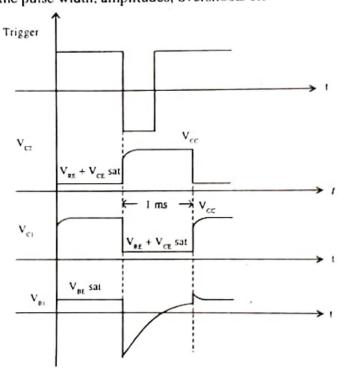


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#### Procedure

- 1. Test all components and probes before rigging up the circuit.
- Switch ON V<sub>cc</sub> supply and verify Q<sub>i</sub> is in OFF state and Q<sub>i</sub> is in ON state. V<sub>ci</sub> should be high and V<sub>ci</sub> should be low.
- 3. Switch ON trigger supply, Trigger should have sufficient amplitude.
- Observe the collector and base waveforms of both transistors. Note down all aspects of the waveforms such as the pulse width, amplitudes, overshoots etc.





#### **Reference**

Electronics Lab Manual Volume I, K.A. Navas, Rajath Publishers