DEPARTMENT OF PHYSICS

MAR THOMA COLLEGE FOR WOMEN, PERUMBAVOOR

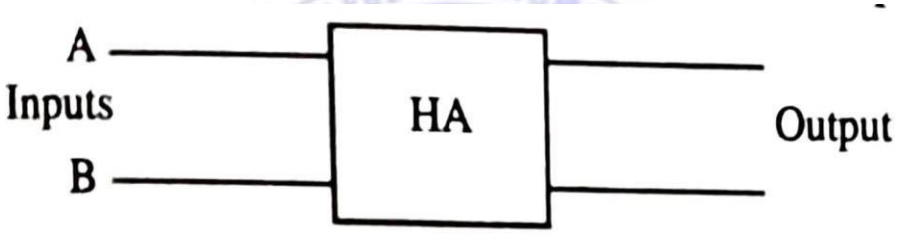
REALIZATION OF HALF ADDER USING GATES VERIFICATION OF TRUTH TABLE

A half adder is a digital circuit that performs the basic arithmetic operation of adding two single-bit numbers and producing the sum as an output

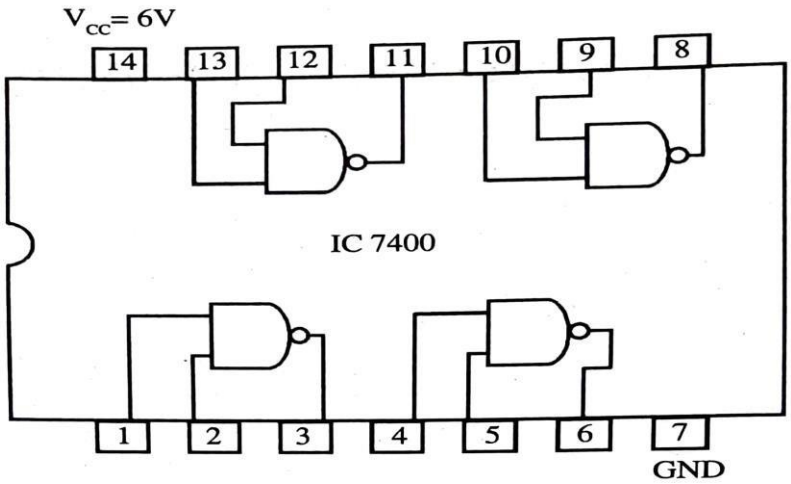
Aim

To construct half adder (HA) and to verify its truth table.

Half adder (HA) is a logic circuit for the addition of two one-bit binary numbers. Half adder gives a sum (S) and Carry (C)on its output.



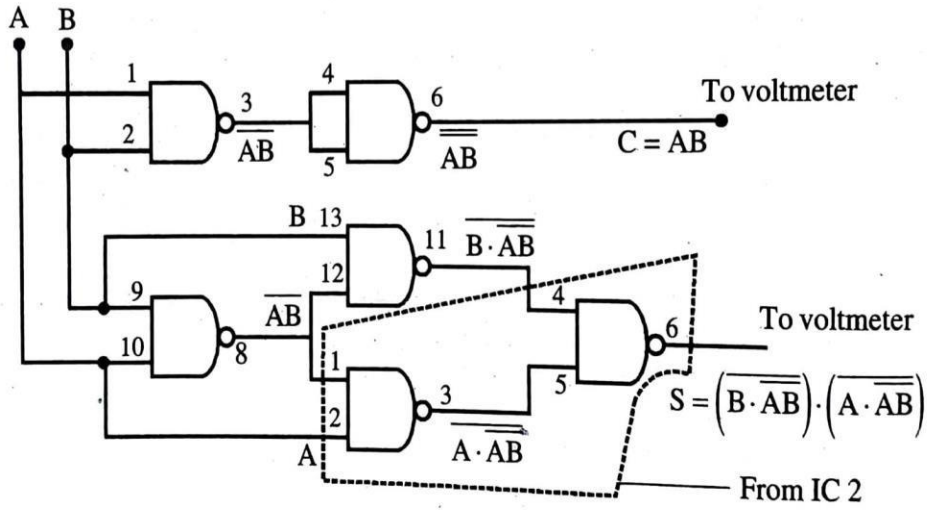
The logic circuit of HA is



A and B are inputs. The carry (c)output is produced with an AND gate. The sum (S) output is produced with an exclusive – OR gate its truth table is

Inputs		Outputs	
A	B	$S = (\bar{A}B + A\bar{B})$	$C = AB$
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

For connection two IC 7400 are used. Because one quad IC consists of only four NAND gates. Between S and ground of IC 2 sum is measured and between C and ground of IC 1 carry is measured using a voltmeter (0-12V). The voltmeter is connected in between pins 6 and 7.



Inputs		Sum	Carry
A	B	S	C
0	0	0	0
0	6V	6V	0
6V	0	6V	0
6V	6V	0	6V

Result

The half adder using NAND gates is constructed and its truth table is verified.

References

- Experimental Physics – II, For Fifth & Sixth Semester, BSc Degree Programme, Dr.P. Sethumadhavan, Prof. K.C. Abraham, Prof. Meppayil Narayanan, Prof. Philipson C Philip, **Manjusha Publications**
- https://youtu.be/S91WnV2wCbA?si=5Dk7SaKXS3yKyODl