



DEPARTMENT OF PHYSICS  
MAR THOMA COLLEGE FOR WOMEN, PERUMBAVOOR

**GATES – OR, AND, NOT – VERIFICATION OF TRUTH TABLES**

Gates are fundamental building blocks of digital logic circuits. Three commonly used gates are the OR gate, the AND gate, and the NOT gate. The truth tables for these gates can be verified to ensure their proper functioning.

**Aim**

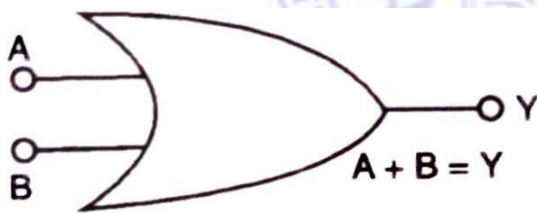
To fabricate OR, AND and NOT gates using diodes and transistors and verification of truth tables.

**Apparatus**

Two diodes, two batteries of 5V each, one resistance of about 1 k $\Omega$ , a bread board, a transistor (BC 107), 1k $\Omega$  and 2.2k $\Omega$ .

**Theory**

OR gate: In this logic gate there are two inputs A and B which operates in such a way that the output is high if one of the two inputs or both inputs is high. The symbol and truth table are given below.



(a) Symbol of OR gate

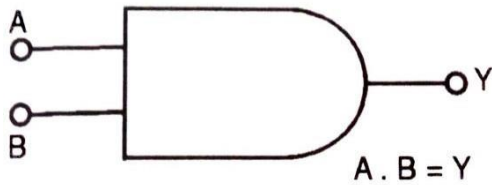
INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table for OR gate

AND gate: In this logic gate there are two inputs A and B which operate in such a way that the output is high (ie ) only when both the inputs are high. The symbol and truth table are given below



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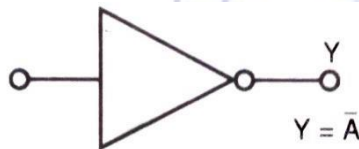


INPUT		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(a) Symbol of AND gate

(b) Truth table of AND gate

NOT gate: This gate is also called as an inverter. The output in this gate is high (i.e.,1) when the input is low (i.e.,0). Also when the input is high (i.e.,1) the output is low (i.e.,0). The symbol and truth table for NOT gate are given below.



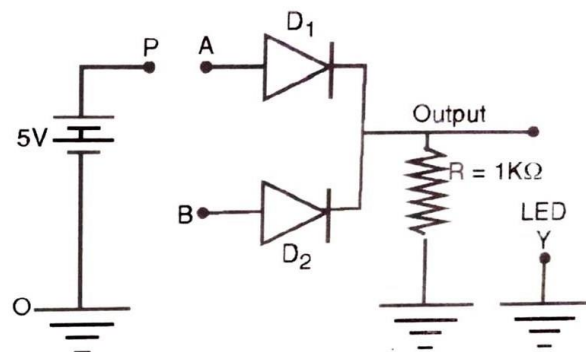
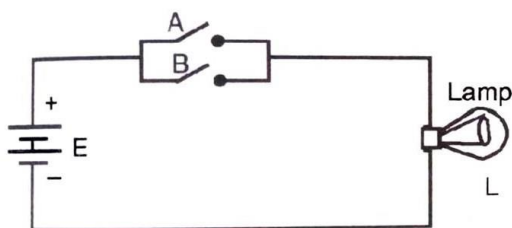
INPUT	OUTPUT
A	Y
0	1
1	0

For NOT gate. (a) Symbol of NOT gate

(b) Truth table of NOT gate

**Procedure**

I. Realisation of OR gate (circuit diagram)





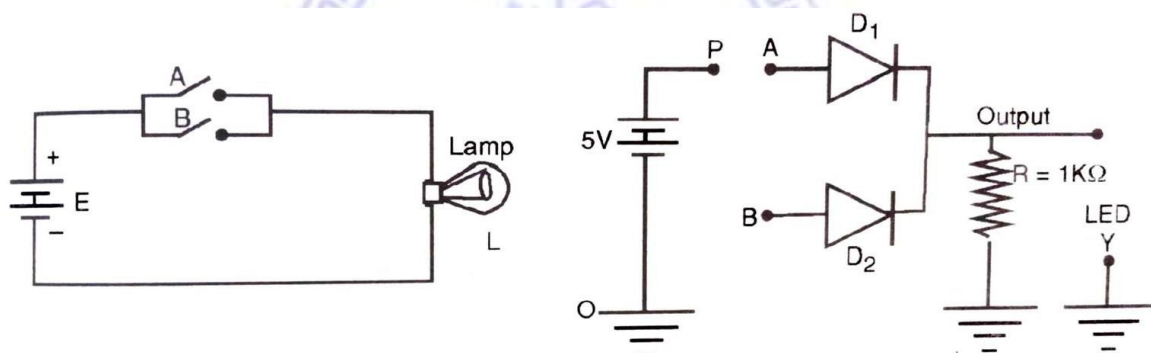
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Make the connections as shown in the figure in a bread board. Logic level whether high or low in the output is indicated by use of LED.

Using the above circuit proceed as follows

1. Connect A and B both to 0 such that both the inputs are low (i.e. 0) and observe the output whether it is higher or low. If it is low the LED does not glow, if it is high LED glows. Record it as 1 if it is high and zero if it is low.
  2. Connect A to 0 and B to P such that A is low and B is high. Record the output Y whether it is high or low. If it is high LED glows on the other hand LED does not glow.
  3. Connect A to P and B to 0 such that A is high and B is low and observe the output Y. Record it as 1 if it is high (LED glows), zero if it is low (LED does not glow).
  4. Connect A to P and B also to P such that both inputs A and B are high. Record the output Y.
- Record the observations in the tabular column.

II. Realisation of AND gate (circuit diagram)



Make the connections as shown in figure in a bread board. Logic level whether high or low in the output is indicated by use of LED in the output.

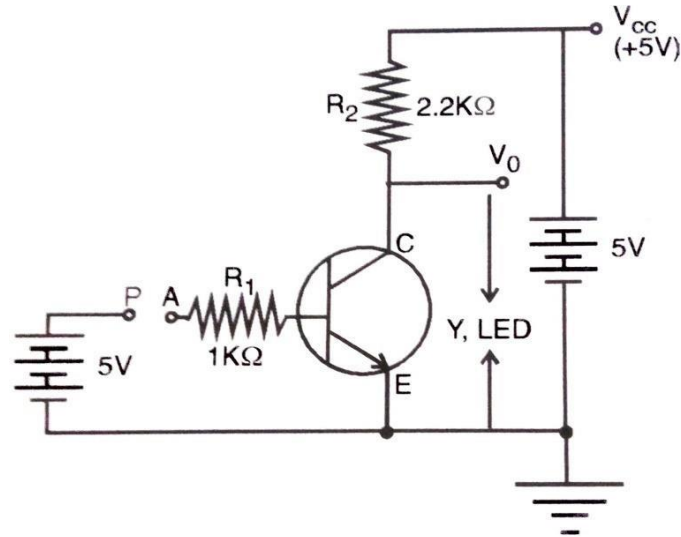
Using the above circuit proceed as follows

1. Connect A and B both to 0 such that both the inputs are low and observe the output whether it is high or low. Record it as 1 if it is high (LED glows) and zero (LED doesn't glow) if it is low.
2. Connect A to 0 and B to P such that A is low and B is high. Note the output and record it.
3. Connect A to P and B to 0 such that A is high and B is low. Record the output Y.
4. Connect A to P and B to P both are high and record the output Y.



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III. Realisation of NOT gate (circuit diagram)



Make the connections as shown in figure in a bread board. Logic level whether high or low in the output is indicated by use of LED.

Using the above circuit proceed as follows

1. Connect A to O such that the input is low and observe and record the output Y whether it is high or low. Record high as 1 (LED glows) and low as zero (LED doesn't glow).
2. Connect A to P such that the input is high (i.e. 1) and record the output Y. Record high as 1 (LED glows) and low as zero (LED doesn't glow).

Record the observations in the tabular column.



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**Observations and tabulations**

Observations for OR gate

INPUT		OUTPUT
A	B	Y

Observations for AND gate

INPUT		OUTPUT
A	B	Y



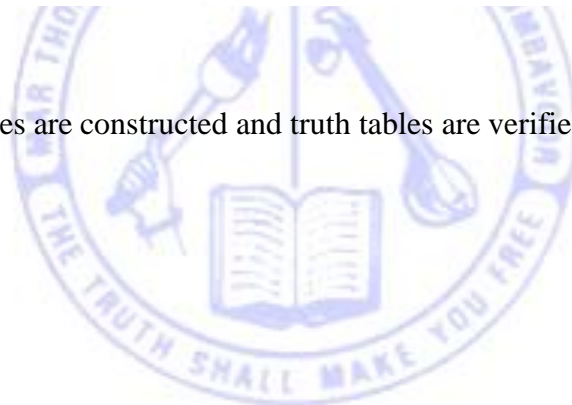
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Observations for NOT gate

INPUT	OUTPUT
A	Y

**Result**

OR, AND and NOT gates are constructed and truth tables are verified.



**References**

Experimental Physics – II, For Fifth & Sixth Semester, BSc Degree Programme, Dr.P. Sethumadhavan, Prof. K.C. Abraham, Prof. Meppayil Narayanan, Prof. Philipson C Philip, **Manjusha Publications**



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