COMMON SOURCE JFET AMPLIFIER

Aim To design, set up and plot the frequency response of a common source JFET amplifier.

Components and equipments required JFET, dc source, capacitors, resistors, bread board, signal generator and CRO.

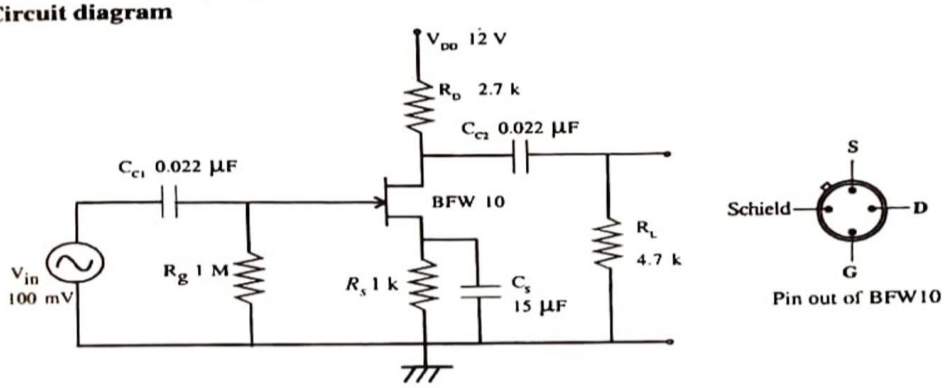
Theory Junction field effect transistor (JFET) is a unipolar voltage controlled device. The drain current is controlled by the voltage at gate. Like transistors, JFET amplifiers can also be set up in three configurations namely, common drain, common source and common gate. Common source configuration is similar to common-emitter configuration of transistor.

JFETs can be biased as voltage divider bias or self bias. A self bias circuit is shown in the circuit diagram. Self bias maintains drain current and g_m relatively constant. Constant g_m results in a constant voltage gain. The design of the circuit is done in such a way that the gate to source junction is reverse biased. The reverse biased junction provides high input impedance. The applied input voltage slightly changes the gate potential and in turn, the drain current varies. The output voltage varies with the drain current.

Procedure

1. Set up the circuit on breadboard. Check the dc conditions and apply the input sinusoidal signal from signal generator to the gate.
2. Obtain the amplified output. Take the output amplitude for various frequencies at the input.
3. Plot the frequency response. Find the bandwidth of the FET amplifier.

Circuit diagram



Design Output requirements Gain = 10.

Selection of FET Select JFET BFW 10 or BFW11.

Specifications of BFW10/11 N-channel JFET, $I_D = 2$ mA, $R_O = 40$ k and $g_m = 2.5$ mA/V

DC biasing conditions $V_{DD} = 12$ V, $V_{GS} = -2$ V , $V_{RD} = 45$ % of $V_{DD} = 5.4$V.

Design of R_S $R_S = V_{RS}/I_S = V_{RS}/I_D$. But $I_D = I_S = 2$ mA and

$V_{RS} = V_G - V_{GS} = 0 - (-2\text{ V}) = 2$ V.

Substituting these values, we get $R_S = 1$ k.

Design of R_D $V_{RD} = I_D R_D = 5.4$ V. From this, we get $R_D = 2.7$ k. Use 2.7 k std.

Design of Rg Select $R_g = 1$ MΩ to make gate current negligible.

Design of R_L Gain of CS amplifier $A = g_m(R_D \| R_L)$. Since required A = 10, we get $R_L = 4.7$ k.

Design of blocking capacitors C_{C1} and C_{C2} Impedance of the coupling capacitor $X_{C1} \le R_g/10$.

Then $X_{C1} \le 0.1$ MΩ. So, $C_{C1} \ge 1/2\pi f_L \times 0.1 \times 10^6 = 0.016$ µF. Use $C_{C1} = 0.022$ µF.

Take $C_{C1} = C_{C2} = 0.022$ µF.

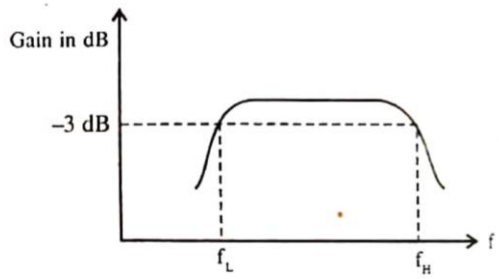
Design of bypass capacitor C_S Take $X_{CS} = R_S/10$ at 100-Hz to bypass this frequency.

Then $X_{CE} \le 100\ \Omega$. So, $C_{CE} \ge 1/2\pi f_L \times 100 = 16$ µF. Use $C_{CE} = 15$ µF std.

Observation $V_{in} = 100\,mV$

f in Hz	V_O in Volts	Gain in dB

Graph



Result Band width = ...Hz

Reference

Electronics Lab Manual Volume I, K.A. Navas, **Rajath Publishers**